

**WHAT IS CLAIMED IS:**

1. A thin film transistor array panel for a liquid crystal display, comprising:

a gate wire including gate lines formed in a horizontal direction;

a data wire including data lines formed in a vertical direction, wherein said data wire intersects and is insulated from said gate wire;

a pixel electrode formed in a pixel defined by an intersection of the gate line and the data line, receiving image signals through the data line;

a storage wire including storage electrode lines and storage electrodes connected to the storage electrode lines, wherein the storage wire forms a storage capacitance by overlapping said pixel electrode; and

a storage wire connection line at least connecting the storage wires to a neighboring pixel.

2. The thin film transistor array panel of claim 1, further comprising a redundant repair line each end of which overlaps the storage wire of a neighboring pixel.

3. The thin film transistor array panel of claim 2, wherein the storage wire connection line is formed on the same layer as said pixel electrode.

4. The thin film transistor array panel of claim 1, wherein said redundant repair line is formed on the same layer as said data wire.

5. The thin film transistor array panel of claim 1, wherein said storage wires are formed on the same layer as said gate wire.

6. The thin film transistor array panel of claim 1, wherein said storage

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21

wire overlaps an edge portion of the pixel electrode.

7. The thin film transistor array panel of claim 1, wherein the pixel electrode has a plurality of connected squares with rounded corners, an opening pattern in a square shape, saw-toothed shape or cross shape to align liquid crystal molecules in a multi-domain configuration.

8. A thin film transistor array panel for a liquid crystal display, comprising:

an insulating substrate;

a gate wire formed on the insulating substrate, wherein said gate wire includes a gate line formed in a horizontal direction and transmitting a scanning signal, and a gate electrode connected to the gate line;

a storage wire formed on the insulating substrate, wherein said storage wire includes a storage electrode line formed in a horizontal direction, and a storage electrode connected to the storage electrode line;

a gate insulating layer covering said gate wire and said storage wire;

a semiconductor layer formed on the gate insulating layer and made of semiconductor material;

a data wire including a data line formed in a vertical direction, a source electrode connected to the data line and extended on the semiconductor layer, and a drain electrode extended on the semiconductor layer and separated from the source electrode with respect to the gate electrode, wherein the data line defines a pixel of a matrix array by intersecting the gate line;

a passivation layer covering said semiconductor layer;

a pixel electrode formed in the pixel and electrically connected to the drain electrode, wherein said pixel electrode forms a storage capacitance by overlapping the storage wire; and

a storage wire connection line at least connecting the storage wire of neighboring pixels.

9. The thin film transistor array panel of claim 8, wherein the pixel electrode and the storage wire connection line are formed on the same layer as each other.

10. The thin film transistor array panel of claim 7, wherein the pixel electrode and the storage wire connection line are formed on said passivation layer.

11. The thin film transistor array panel of claim 6, further comprising a redundant repair line each end of which overlaps the storage wires of a neighboring pixel and which is formed on the same layer as the data wire.

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